CHAPTER 7
COUNTERS AND REGISTERS

7.0 INTRODUCTION

The subjects for this chapter are counters and registers. As you may recall from Chapter 5, counters and registers are composed of flip-flops. Counters will count the number of pulses applied to the count input. Registers are used to store and manipulate numbers. You will learn about different types of counters and registers, and the implementation of counter and register circuits.

7.1 OBJECTIVES

Upon completion of this chapter you should be able to:

- Discuss the operation of ripple counters.
- Explain the operation of MOD counters.
- Implement UP/DOWN counters.

- Explain registers and their applications.
- Build counter and register circuits.

7.2 DISCUSSION

This chapter covers the uses of counters and registers. This study will begin with a discussion of several different types of counters. Subsequent sections will deal with using registers.

7.2.0 Ripple Counters

The simplest type of counter you will encounter is the ripple counter. A ripple counter is formed with a series of cascaded flip-flops. The flip-flops are connected as toggles and the output of one stage feeds the clock input of the next stage. Two examples of two-digit ripple counters are shown in Figure 7–1.

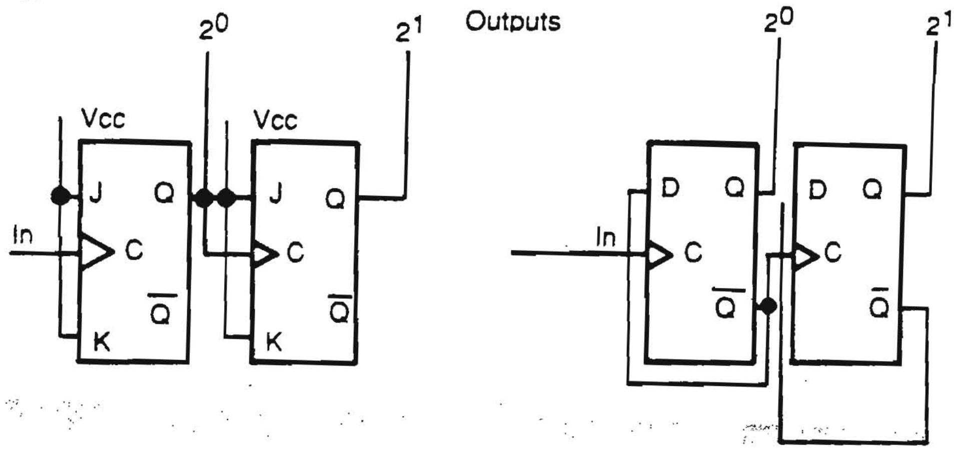


FIGURE 7-1. Examples of Ripple Counters.

8 4 2 1

Notice that either D or J-K flip-flops can be used to implement counters. Also notice that the output frequency of each counter stage is one-half the frequency of the input clock.

The counters in Figure 7-1 are both binary counters capable of four output states. Ripple counters get their name from the way that clock pulses, which are the stage outputs, ripple through the flip-flops forming the counter. The number of distinct counter stages is 2^N, where N is the number of flip-flops or stages. The maximum number that a counter of this type can represent is $2^{(N-1)}$. So, the counters in Figure 7-1 can have four states and represent numbers up to three.

When changing from 11 to 00 this type of counter requires that each flip-flop making up the counter change state before the count is completed. This is the most active transition for the counter and can be used to calculate the maximum count rate by the formula shown in Figure 7-2. Each stage making up the counter has a propagation delay time; that is, the time between the input pulse to the stage and the stage output response.

$$1/f = T = N \cdot TP + TS$$

where: N = number of flip-flops

TP = propagation delay of one flip-flop

TS= strobe time

FIGURE 7-2. Count Rate Formula.

A strobe is a delayed clock pulse which is used to inhibit the counter decoder circuitry while the flip-flops that make up the counter are changing states. The strobe is used to prevent the display of glitches while the counter changes states. Figure 7-3 shows the relationship between clock and strobe pulses.

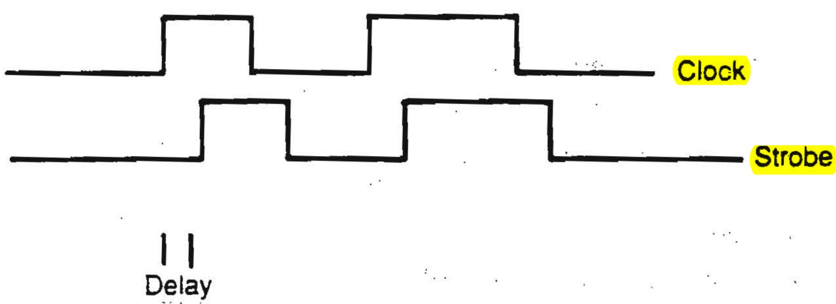


FIGURE 7-3. Clock and Strobe Pulses.

For the counters shown the maximum counting frequency is 6.67 MHz assuming 50 nS. for both the gate delay and strobe times.

7.2.1 MOD Counters

The counters that have been studied to this point are all binary counters. They can count a number of steps which are an integral power of two. The number of steps that a counter can count is known as the modulus or MOD of the counter. The counters in Figure 7-1 were modulus 4 counters.

You can build counters of any MOD from binary ripple counters by detecting the number of the modulus of the counter and then resetting all of the flip-flops in the counter. For example, to make a modulus 3 counter from the circuit in

Figure 7-1 you need to detect when the output is three and then reset both of the counter flip-flops. While it is true that the counter will have a 3 output while the counter decoder circuitry switches, this state can be masked by using a strobe to enable the decoding circuits. The output of the counter will then appear as the sequence 0, 1, 2, reset.

This style of circuit, known as a premature reset counter, can be used to make a counter of any MOD. MOD counters can be cascaded (output of one stage feeding the input of the next stage) to form counters of a greater modulus. The MOD 4 counter of Figure 7-1 can be connected with a MOD 3 counter to form a MOD 12 counter. Notice that this circuitry can be connected two ways in that either counter can be used to and from the first counter stage.

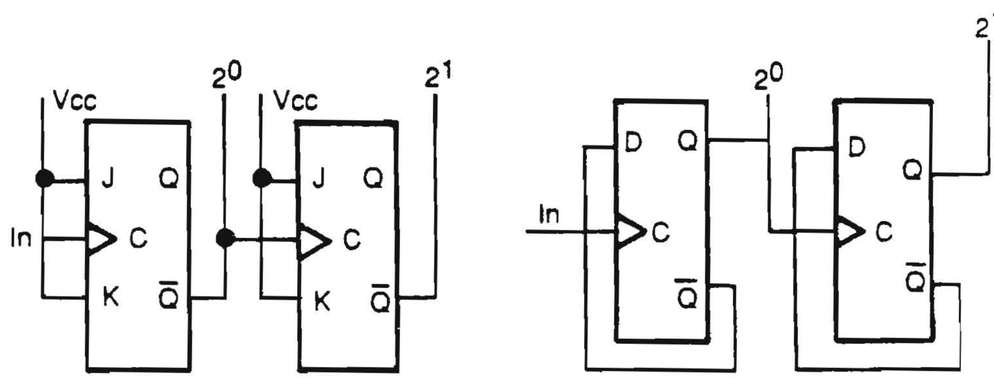
This technique is used in the 7490 TTL IC which has MOD 2 and MOD 5 counters which can be connected to form a decade or MOD 10 counter. At this point you have the knowledge to construct counters of any modulus.

7.2.2 Down Counters

The counters studied to this point have all been up counters. Some applications require the ability to count down. A down counter can be implemented with the same circuitry used for ripple up counters. By connecting the complement output instead of the true output to the next counter stage J-K flip-flops will form down counters.

Likewise, the true instead of the complement output is connected to the next counter stage to form down counters from D flip-flops. Down counter circuits are shown in Figure 7-4.

FIGURE 7-4. Examples of Down Counters.



7.2.3 Parallel Counters

Parallel or synchronous counters are implemented so that each stage of the counter changes state at the same time. This is accomplished by having the clock lines to all counter stages connected in parallel.

The advantage of this configuration is that only one gate delay is required for the counter stages to change state. While some additional gating and decoding circuitry is frequently needed with parallel counter circuits, the switching time required for the counter doesn't increase proportionally with counter size as is the case with the ripple counters studied previously. An example of a simple parallel counter is shown in Figure 7-5.

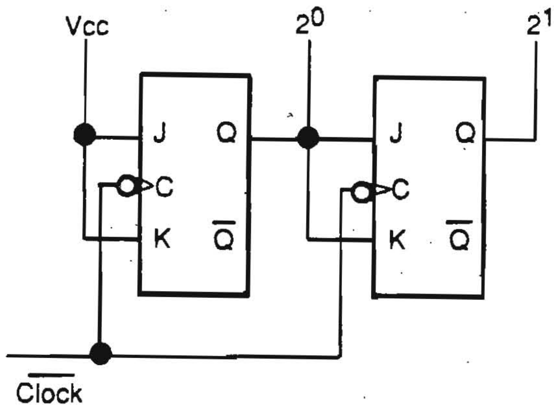


FIGURE 7-5. Parallel Counter Circuit.

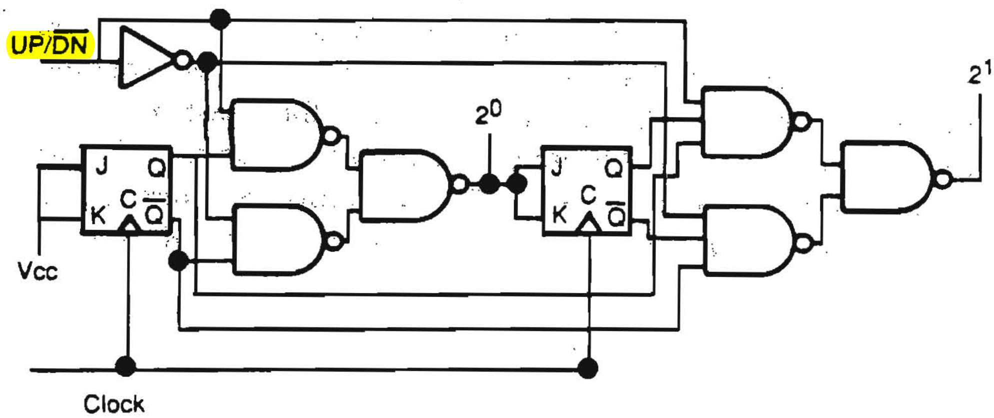
The counter shown in Figure 7-5 is an up counter. A down counter can be constructed using the same gates with the complement output used for the output of each stage.

For synchronous counters, each stage past the second stage requires one more AND gate to drive the J and K inputs of the next stage and the number of inputs into the AND is one less than the stage that the output of the gate drives. For example, the J and K inputs of the third stage are driven by a two-input AND gate. The inputs to the AND gate are the true outputs of the previous stage.

7.2.4 Parallel UP/DOWN Counter

Many applications exist that require the ability to count up or down. While this could be accomplished by having two separate counters, such a configuration would be a waste of circuitry. With some additional logic circuitry, parallel counters can be made to count either up or down. An example of such a circuit is shown in Figure 7-6.

FIGURE 7-6. Parallel Up/Down Counter.



Notice that the circuitry routes the true and complement outputs of each counter stage to perform the selected type of count. Also note that the carry function is performed by the outputs of the first J-K flip-flop being directly fed to the gating circuitry of the next stage.

Each successive stage will contain the same number of gating circuits (3) with the paired gates needing one more input for each stage. This type of circuit is known as a fully synchronous up/down counter.

The carry function may be performed in a simpler manner by feeding the previous lower order bit directly to the paired gates of the next stage's gating circuitry. A circuit constructed in this manner is known as ripple carry synchronous up/down counter. The advantage of this type of circuit is that the paired gates in the gating circuitry are simpler gates. The ripple carry counter will count faster than a ripple counter and slower than a fully synchronous counter.

7.2.5 Presetable Counters

The counters studied up to this point count up or down from zero. In order to allow the ability to start the count at other numbers, flip-flops with preset and clear inputs are used to form the counter stages. An example of this type circuit is shown in Figure 7-7.

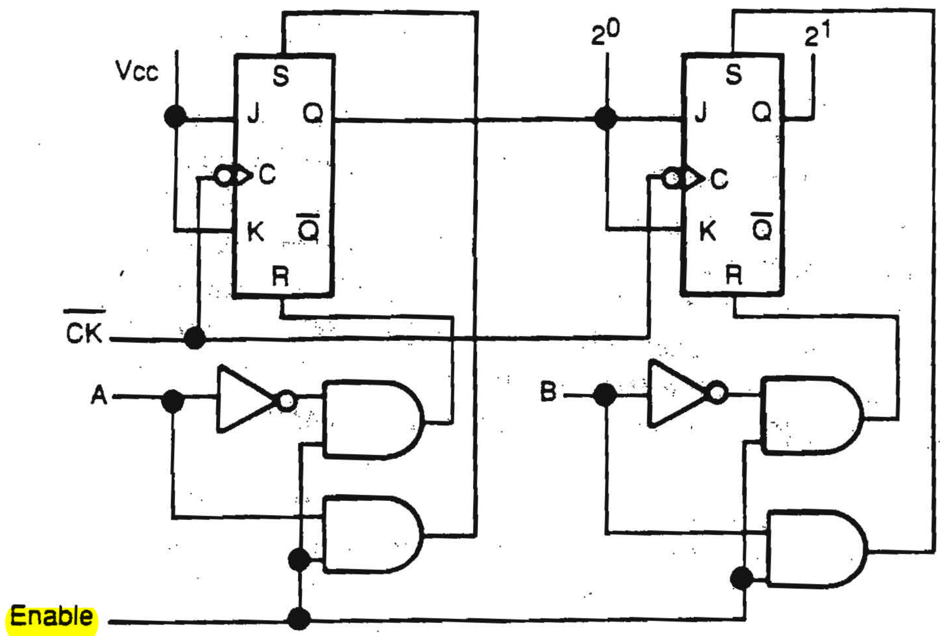


FIGURE 7-7. Presetable Counter.

This circuit will count like the other counters studied but can begin the count at any number. When the ENABLE input is HI, the A and B inputs will determine the state of the counter outputs by acting on the SET and RESET inputs of the J-K flip-flops which make up the counter.

7.2.6 IC Binary UP/DOWN Counter

Constructing counters of any size from discrete flip-flops is tedious business at best. For this reason, IC counters in a variety of prepackaged types have been developed.

One example of an IC counter is the 74193 synchronous 4-bit up/down counter. This versatile circuit is made of about 55 gate equivalents and can count at frequencies up to about 32 MHz. The 74193 is presettable via use of the load input in conjunction with the A-D data inputs. This counter also has a clear input which resets all outputs. 74193s are provided with borrow inputs and carry outputs so that they can be easily cascaded without using external circuitry. Figure 7-19, in the laboratory section, shows a logic diagram for the 74193.

7.2.7 Counter Decoding

The counters covered to this point have had binary outputs. While this is generally satisfactory, many applications require that some type of decoding of the binary count be performed. Frequently, the output of a four-bit binary counter will be converted to a decimal output for easier use by people.

Recall from Chapter 4 that decoders are constructed from

AND and NOT gates. You have already learned to construct simple decoders.

The only additional consideration for decoding counters beyond that of decoding other binary outputs is that the enable line for the decoding circuitry may need to be slightly delayed from the counter clock pulse. If this is not done, false counts can be displayed and the decoder can operate erratically. For this reason, a strobe signal, which is a slightly delayed clock signal, is often used to enable the decoder circuits. Counters can also be decoded by IC decoders covered in a later chapter.

7.2.8 Shift Registers

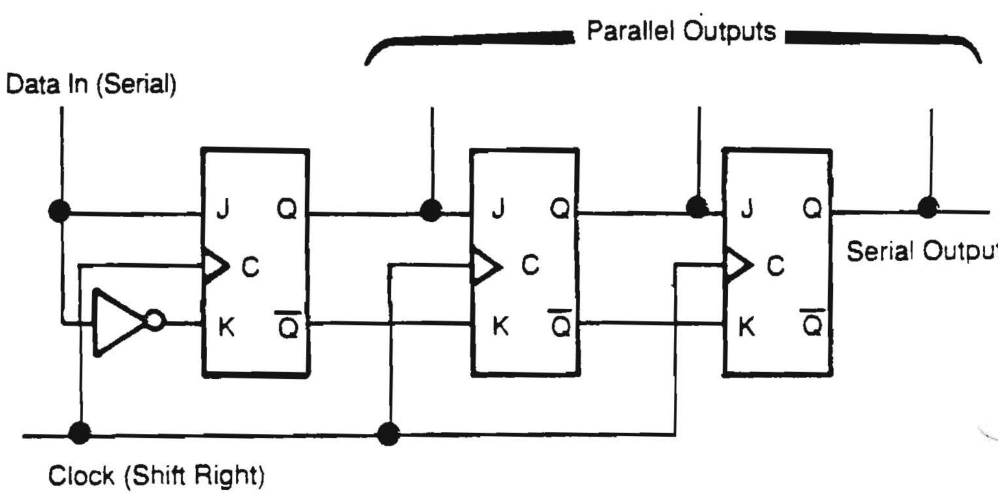
Shift registers are specialized memory systems composed of flip-flops or other types of memory cells. The distinguishing feature of shift registers is that data can be transferred on command from one cell to the adjacent memory cell as many times as needed.

The simplest shift registers will transfer one data bit in for each clock cycle until the register capacity is reached. At this time the register contents may be sampled.

More complex registers will allow direct sampling of each output stage so that the register contents can be examined on each clock cycle. Other registers allow parallel loading where the entire register is loaded at once.

A special type of shift register known as the universal shift register will shift entries left or right, and input or output data serially or parallel. Shift registers may be constructed from either J-K flip-flops as shown in Figure 7-8 or from D flip-flops as shown in Figure 7-9.

FIGURE 7-8. "J-K" Flip-flop Shift Register



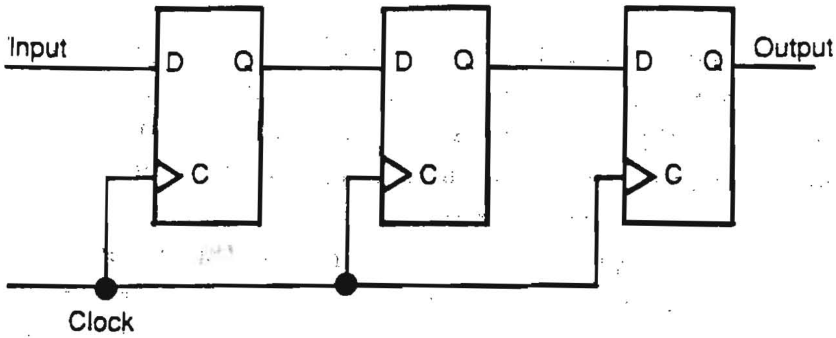


FIGURE 7-9. "D" Flip-flop Shift Register.

The single data input of the shift register in Figure 7-8 is known as a single rail input. If the J and K inputs are used as separate data inputs then the shift register is said to have a dual rail input.

Likewise if the shift register uses both the true and complement outputs the circuit is called a dual rail output circuit. Of course if only one of the outputs is used then the circuit is described as having a single rail output. Note that the output of the J-K shift register shown can be either serial or parallel. Shift registers can be classified as :

a. Serial-in/serial-out: SISO

b. Serial-in/parallel-out: SIPO

c. Parallel-in/serial-out: PISO

d. Parallel-in/parallel-out: PIPO

All parallel input registers can be operated as serial input registers and the same is true for output. The reverse situation is not true in that serial input registers cannot be operated as parallel input registers.

7.2.9 Johnson Counter

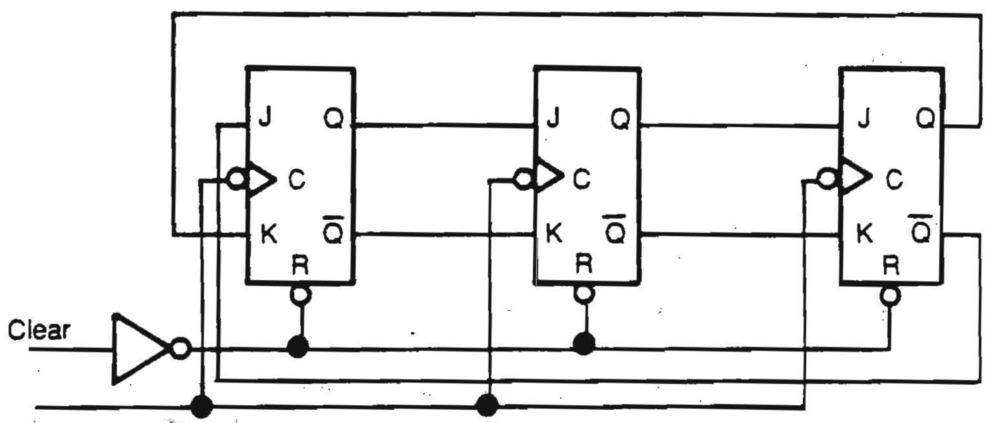
Shift registers can be used to form a special kind of counter known as a ring counter. A ring counter works by loading a binary ONE into the input flip-flop of a shift register and tying the register output to the input. When the register is clocked the ONE will move through the register one cell at a time. After a number of clock pulses equal to the number of cells in the register, the ONE will circulate back to the input flip-flop.

This allows a form of counting. This type of counter uses more flip-flops than required to perform the count. For example, three flip-flops configured as a ring counter can have only three states or counts while a binary counter with three flip-flops can count eight states when properly decoded.

The advantage of the ring counter is that no decoding is required to determine the count. The ring counter has 2^N-N disallowed states where that N is the number of flip-flops. A special type of ring counter is the Johnson counter.

The Johnson counter has the output inverted before it is feedback to the input so that the maximum count is 2•N with N being the number of flip-flops. This, of course means that the Johnson counter has 2^N-2•N disallowed states. The Johnson counter makes better use of the flip-flops than a simple ring counter. The truth table and schematic for a 3-flip-flop Johnson counter are shown in Figure 7-10.

FIGURE 7-10. Johnson Counter.



A Johnson counter can be decoded by using a two-input AND for each decoded output.

7.2.10 Integrated Circuit Registers

It should not surprise you that a variety of shift registers are available as ICs. These circuits are much easier to use than registers constructed from discrete components. They also offer significant performance advantages over discretes. All of the register types studied are available as either TTL or CMOS ICs. The 74174 IC is a HEX D-TYPE flip-flops with clear IC, it can be connected to form a parallel-in/parallel-out shift register. The logic diagram for the 74174 is shown in Figure 7-11.

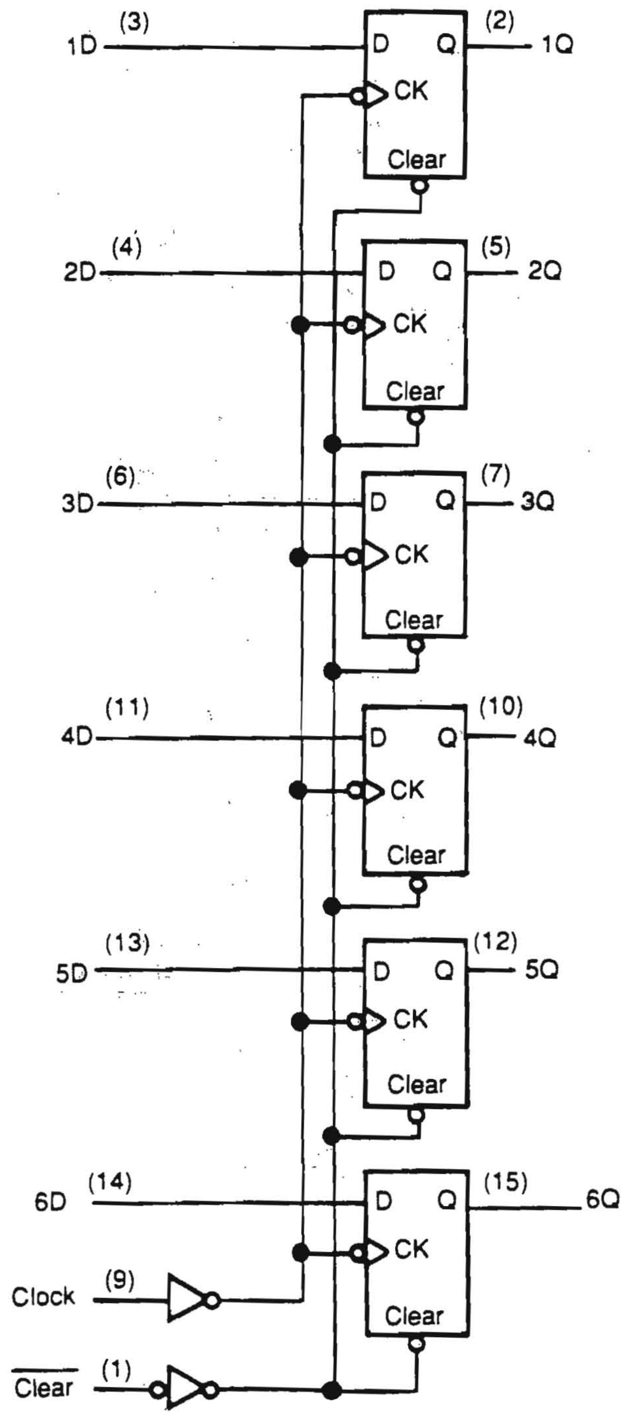
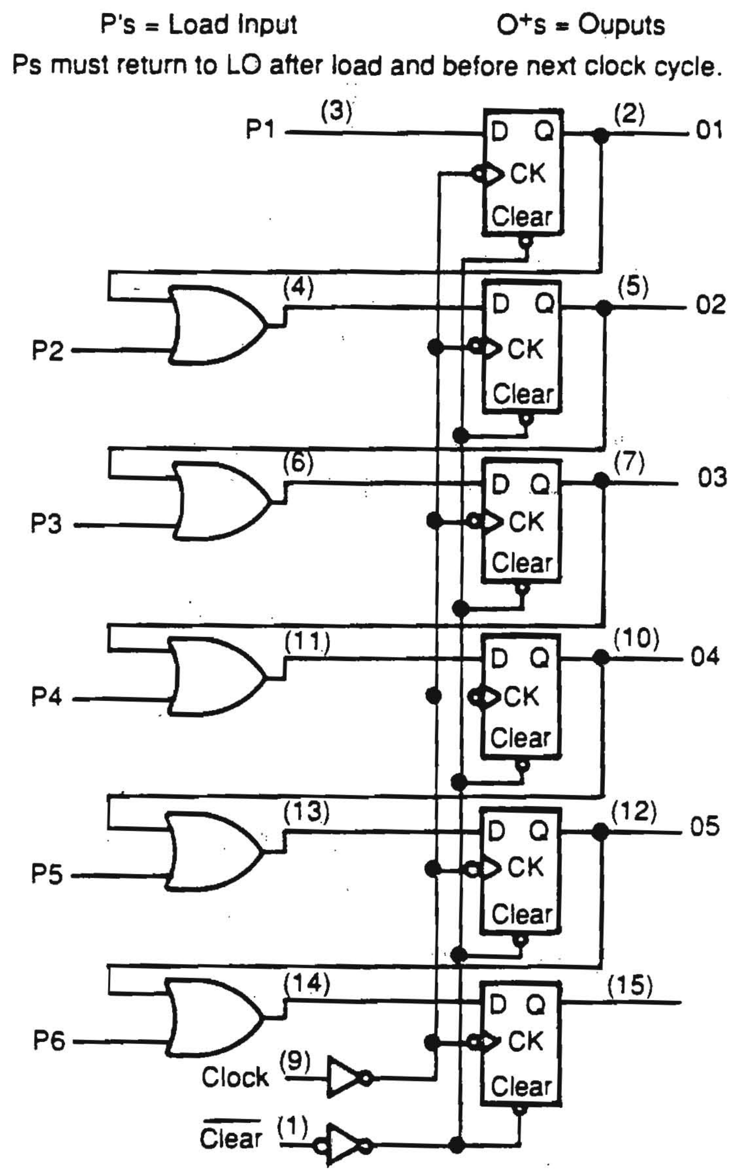


FIGURE 7-11. 74174 Logic Diagram.

The schematic for the PIPO shift register constructed from a 74174 is shown in Figure 7-12. This type of circuit does not have a true parallel load capacity in that all of the flip-flops in the register must be cleared before the new parallel data is loaded.

FIGURE 7-12. 74174 PIPO Shift Register.



The 74174 is also quite versatile in that it may be connected as a SISO, SIPO (Figure 7-9), or PISO shift register since the interconnection between flip-flops is not pre-determined.

Another type of shift register, the 7494, provides a SISO capability. The 7494 also has a controlled parallel preset capability. The 7494 can be used as a shift right SISO register or as a parallel to serial converter. The logic diagram of the 7494 is shown in Figure 7-13.

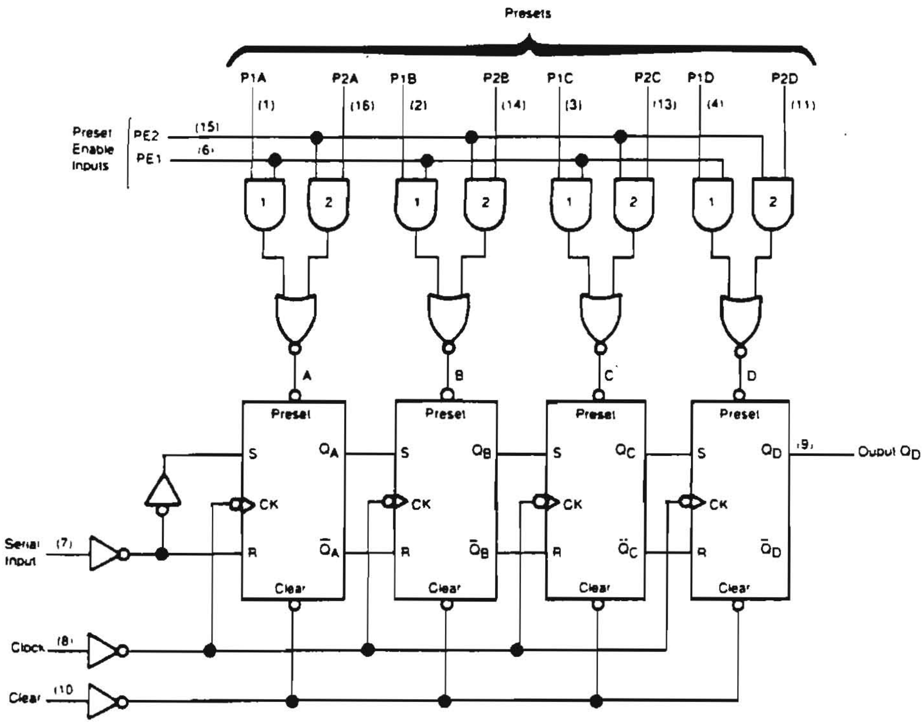


FIGURE 7-13. 7494 Logic Diagram.

The 7494 may be parallel loaded by first clearing the register then loading the data using the preset inputs. Notice that this register is composed of RS flip-flops and the data is transferred on the positive-going edge of the clock pulse.

A PISO capability is provided by the 74165 IC. These ICs are eight bit serial shift registers that shift the data from Qa toward Qh. A LO level on the shift/LD input enables the eight input data lines. These registers have gated clock inputs and complementary outputs for the eighth bit. The logic diagram for the 74165 is shown in Figure 7-14.

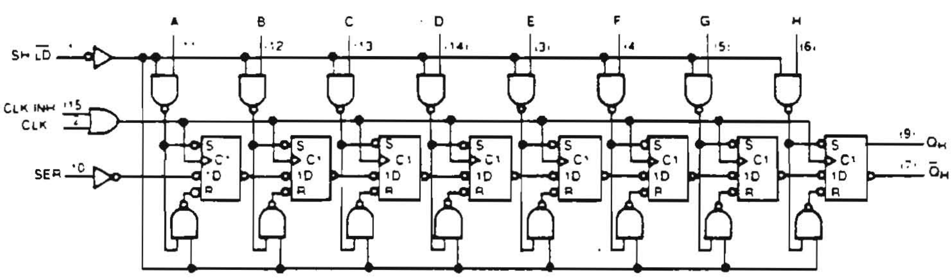


FIGURE 7-14. 74165 Logic Diagram.

The last type of register discussed here will be the 74164. The 74164 provides a SIPO capability. These registers feature gated serial input and an asynchronous clear capability. The gated A and B inputs permit complete control of incoming data as a LO on either input inhibits entry of new data and resets the low order flip-flop of the register on the next clock pulse.

Data transfer occurs on the LO to HI transition of the clock pulse. The 74164 has eight parallel output data bits. The logic diagram of the 74164 is shown in Figure 7-15.

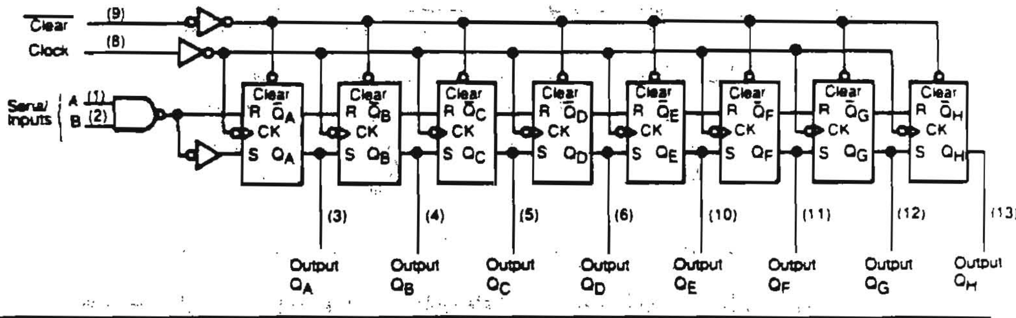


FIGURE 7-15. 74164 Logic Diagram.

7.3 SUMMARY

In this chapter you learned about counters and shift registers. You studied ripple and synchronous binary counters. You also studied up and down counters, counters of various modulus and presettable counters.

Decoding counter outputs to provide outputs in forms other than binary was discussed. You have learned about shift registers. You have seen shift registers used to form ring counters, such as the Johnson counter. You studied IC registers sufficiently to learn the circuitry used to implement all common types of shift registers.

7.4 REVIEW QUESTIONS

1. Explain what is meant by a ripple counter.

2. What is the modulus of a counter?

3. What is the difference in the circuit connections for up and down counters?